WHAT IS CLAIMED IS:

1. A wiring method for placing interconnection lines for a plurality of bits in parallel two-dimensionally or three-dimensionally in layout design of a semiconductor integrated circuit,

wherein the interconnection lines for a plurality of bits are placed in an ascending or descending order of the bits,

interconnection lines for bits of ordinal numbers equal to or more than a predetermined ordinal number are placed adjacent to each other at a predetermined spacing, and

interconnection lines for bits of ordinal numbers less than the predetermined ordinal number are placed adjacent to each other at a spacing exceeding the predetermined spacing.

2. A wiring method for placing interconnection lines in parallel two-dimensionally or three-dimensionally in layout design of a semiconductor integrated circuit,

wherein a signal change frequency at which a signal propagating through an interconnection line changes per unit time is determined for each of the plurality of interconnection lines by estimation or simulation, and

the plurality of interconnection lines are placed based on the signal change frequency so that interconnection lines having a high signal change frequency and interconnection

lines having a low signal change frequency are adjacent to each other.

3. The method of Claim 2, wherein, in the case of transmitting a signal of a plurality of bits via the plurality of interconnection lines, the plurality of interconnection lines are placed based on the signal change frequency, irrespective of an ascending or descending order of the bits.

4. The method of Claim 2, wherein the plurality of interconnection lines are placed so that interconnection lines having a high signal change frequency are sandwiched by interconnection lines having a low signal change frequency.

5. A wiring method for placing interconnection lines for a plurality of bits in parallel two-dimensionally or three-dimensionally in layout design of a semiconductor integrated circuit,

wherein in placement of the interconnection lines for a plurality of bits, one interconnection line for a bit of an ordinal number equal to or more than a predetermined ordinal number and an interconnection line for a bit of an ordinal number less than the predetermined ordinal number are placed adjacent to each other, and

another interconnection line for a bit of an ordinal number equal to or more than the predetermined ordinal number and another interconnection line for a bit of an ordinal number less than the predetermined ordinal number are placed adjacent to each other, and this placement is repeated.

6. The method of Claim 5, wherein interconnection lines for bits are placed in a descending order from the most significant bit until a bit of the predetermined ordinal number in parallel two-dimensionally at a spacing double a predetermined spacing, and

interconnection lines for bits are placed in an ascending order from the least significant bit in parallel two-dimensionally between the already-placed interconnection lines.

7. The method of Claim 5, wherein the method comprises the steps of:

(1) placing an interconnection line for the least significant bit at a predetermined position;

(2) placing interconnection lines for the two highest-order bits on the right and left sides of the interconnection line for the least significant bit;

(3) placing interconnection lines for the remaining two lowest-order bits on the right and left sides of the

interconnection lines for the two highest-order bits placed in the step (2);

(4) placing interconnection lines for the remaining two highest-order bits on the right and left sides of the interconnection lines for the two lowest-order bits placed in the step (3); and

(5) repeating the steps (3) and (4) until the interconnection lines for all the bits are placed.

8. A wiring method for placing interconnection lines for a plurality of bits in parallel three-dimensionally in n wiring layers ($n \geqq 2$) in layout design of a semiconductor integrated circuit, the method comprising the steps of:

(1) placing an interconnection line for the least significant bit in a predetermined wiring layer;

(2) placing interconnection lines for a plurality of highest-order bits in the same wiring layer as the interconnection line for the least significant bit and a different wiring layer so as to surround the interconnection line for the least significant bit placed in the step (1);

(3) placing interconnection lines for a plurality of remaining lowest-order bits in the same wiring layers as the interconnection lines for a plurality of highest-order bits and a different wiring layer so as to surround the interconnection lines for a plurality of highest-order bits

placed in the step (2); and

(4) repeating the steps (2) and (3) until the interconnection lines for all the bits are placed.

9. The method of Claim 8, wherein the n wiring layers are two wiring layers,

the interconnection line for the least significant bit is placed at a predetermined position of the lower wiring layer in the step (1),

interconnection lines for the three highest-order bits are placed in the lower and upper wiring layers so as to be positioned on the right, left and upper sides of the interconnection line for the least significant bit in the step (2);

interconnection lines for the remaining four lowest-order bits are placed in the lower and upper wiring layers so as to be positioned on the right and left sides of the interconnection lines for the three highest-order bits in the step (3), and

the steps (2) and (3) are repeated until the interconnection lines for all the bits are placed in the step (4).

10. The method of Claim 8, wherein the n wiring layers are two wiring layers,

the interconnection line for the least significant bit is placed at a predetermined position of the upper wiring layer in the step (1),

interconnection lines for the three highest-order bits are placed in the upper and lower wiring layers so as to be positioned on the right, left and lower sides of the interconnection line for the least significant bit in the step (2);

interconnection lines for the remaining four lowest-order bits are placed in the upper and lower wiring layers so as to be positioned on the right and left sides of the interconnection lines for the three highest-order bits in the step (3), and

the steps (2) and (3) are repeated until the interconnection lines for all the bits are placed in the step (4).

11. The method of Claim 8, wherein the n wiring layers are three wiring layers,

the interconnection line for the least significant bit is placed at a predetermined position of the center wiring layer in the step (1),

interconnection lines for the four highest-order bits are placed in the center, lower and upper wiring layers so as to be positioned on the right, left, upper and lower sides of

the interconnection line for the least significant bit in the step (2);

interconnection lines for the remaining six lowest-order bits are placed in the center, lower and upper wiring layers so as to be positioned on the right and left sides of the interconnection lines for the four highest-order bits in the step (3),

interconnection lines for the remaining six highest-order bits are placed in the center, lower and upper wiring layers so as to be positioned on the right and left sides of the interconnection lines for the six lowest-order bits in the step (4), and

the steps (3) and (4) are repeated until the interconnection lines for all the bits are placed.

12. A semiconductor integrated circuit having interconnection lines for a plurality of bits placed in an ascending or descending order of the bits in parallel two-dimensionally or three-dimensionally,

wherein the spacing between interconnection lines for bits of ordinal numbers less than a predetermined ordinal number is larger than the spacing between interconnection lines for bits of ordinal numbers equal to or more than the predetermined ordinal number.

13. A semiconductor integrated circuit having a plurality of interconnection lines placed in parallel two-dimensionally or three-dimensionally,

wherein the plurality of interconnection lines are not placed in an ascending or descending order of a signal change frequency at which a signal propagating through an interconnection line changes.

14. The semiconductor integrated circuit of Claim 13, wherein the plurality of interconnection lines are interconnection lines for a plurality of bits, and

the interconnection lines for a plurality of bits are placed in an order irrespective of an ascending or descending order of the bits.

15. The semiconductor integrated circuit of Claim 13, wherein an interconnection line having a high signal change frequency is sandwiched by two interconnection lines having a low signal change frequency.

16. The semiconductor integrated circuit of any of Claims 13, 14 and 15, wherein the width of the plurality of interconnection lines is 0.18 μm or less.

17. The semiconductor integrated circuit of any of

Claims 13, 14 and 15, wherein the plurality of interconnection lines are a plurality of address bus lines.

18. The semiconductor integrated circuit of any of Claims 13, 14 and 15, wherein signals propagating through the plurality of interconnection lines are digital signals of an image or voice.

19. A semiconductor integrated circuit comprising:

a plurality of interconnection lines;

a processing circuit for performing predetermined processing and outputting signals of results of the predetermined processing to the plurality of interconnection lines; and

switch means disposed between the plurality of interconnection lines and the processing circuit for changing the order of arrangement of the signals output from the processing circuit so that the signals are not arranged in an ascending or descending order of a signal change frequency and transmitting the signals in the changed order to the plurality of interconnection lines.

20. The semiconductor integrated circuit of Claim 19, further comprising:

a receiver circuit for receiving the signals transmitted

through the plurality of interconnection lines; and

second switch means disposed between the plurality of interconnection lines and the receiver circuit for changing the order of arrangement of the signals transmitted through the plurality of interconnection lines to the ascending or descending order of the signal change frequency and transmitting the signals in the changed order to the receiver circuit.

21. A functional macro having a plurality of terminals to which interconnection lines for a plurality of bits are connected,

wherein the plurality of terminals are placed in an ascending or descending order of the bits,

the spacing between terminals for higher-order bits among the plurality of terminals is set at a predetermined spacing, and

the spacing between terminals for lower-order bits among the plurality of terminals is set at a spacing larger than the predetermined spacing.

22. A functional macro having a plurality of terminals to which interconnection lines for a plurality of bits are connected,

wherein the order of arrangement of the plurality of

terminals does not depend on an ascending or descending order of the bits, but is set based on a change frequency of signals input into or output from the terminals.

23. The functional macro of Claim 22, wherein the plurality of terminals are placed so that a terminal having a high signal change frequency is sandwiched by terminals having a low signal change frequency.

24. The functional macro of Claim 23, wherein terminals for higher-order bits of ordinal numbers equal to or more than a predetermined ordinal number are placed in a descending order from the most significant bit at a spacing double a predetermined spacing, and

terminals for lower-order bits of ordinal numbers less than the predetermined ordinal number are placed in an ascending order from the least significant bit between the terminals for the higher-order bits starting from the side of the terminal for the most significant bit.

25. The functional macro of Claim 23, wherein terminals for given two bits continuous from the least significant position are placed on the inner or outer sides of terminals for given two bits continuous from the most significant position.

26. The functional macro of Claim 25, wherein two terminals for the two highest-order bits are placed on both ends, and

two terminals for the two lowest-order bits are placed on the inner sides of the two terminals for the two highest-order bits.

27. The functional macro of Claim 25, wherein a terminal for the least significant bit is placed on the center of the plurality of terminals placed.

28. A semiconductor integrated circuit comprising:

a functional macro having a plurality of terminals arranged in an ascending or descending order of bits,

other terminals identical in number to the plurality of terminals placed in correspondence with the plurality of terminals, the other terminals being arranged in an order based on a signal change frequency; and

a terminal sorting block for connecting the plurality of terminals of the functional macro to the other terminals.

29. The semiconductor integrated circuit of Claim 28, wherein the functional macro, the other terminals and the terminal sorting block are formed integrally.

30. The functional macro of Claim 22, wherein the functional macro is a memory, an operator or a CPU.

31. A wiring method in layout design of a semiconductor integrated circuit, wherein a plurality of interconnection lines are connected to the plurality of terminals of the functional macro of Claim 23, and

an interconnection line on which a signal changes frequently among the plurality of interconnection lines is sandwiched by two interconnection lines on which a signal changes less frequently.

32. A semiconductor integrated circuit comprising,

two or more functional macros of Claim 23; and

a plurality of interconnection lines for connecting the plurality of terminals of the functional macros to each other,

wherein an interconnection line on which a signal changes frequently among the plurality of interconnection lines is sandwiched by two interconnection lines on which a signal changes less frequently.

33. The semiconductor integrated circuit of Claim 32, wherein three or more functional macros are provided, and

the plurality of interconnection lines are address bus lines for a plurality of bits.

34. The semiconductor integrated circuit of Claim 32, wherein two functional macros are provided, one of the two functional macros being an A/D converter, and

the plurality of interconnection lines are data signal interconnection lines for transmitting a digital signal output from the A/D converter by converting an analog value to a digital value.